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Sheet 1 of 1

Complete if Known

Application Number	09/741,821
Filing Date	December 22, 2000
First Named Inventor	Terry R. Lee
Art Unit	2181
Examiner Name	Not Yet Assigned
Attorney Docket Number	M4065.0406/P406

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U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Document Number Number-Kind Code ² (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Where Relevant Passages or Relevant Figures Appear
WJ	A	4,974,152	11/27/1990	Guiffant et al.	

Technology Center 2100

FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Foreign Patent Document Country Code ³ -Number ⁴ -Kind Code ⁵ (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
WJ	A	WO 99/30240 (PCT/US98/25181)	06/17/1999			
WJ	B	WO 99/19874 (PCT/US98/21449)	04/22/1999			

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OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
WJ	A	YASUHIRO KONISHI et al., "Interface Technologies for Memories and ASICs – Review and Future Direction –", IEICE Transactions on Electronics, Vol. E82-C. No. 3 March 1999.	
WJ	B	ALFREDO MONCAYO et al., "Physical Layer Design of a 1.6 GB/s DRAM Bus", 1999 IEEE.	

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Examiner Signature	W. R. R. R.	Date Considered	4/17/13
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